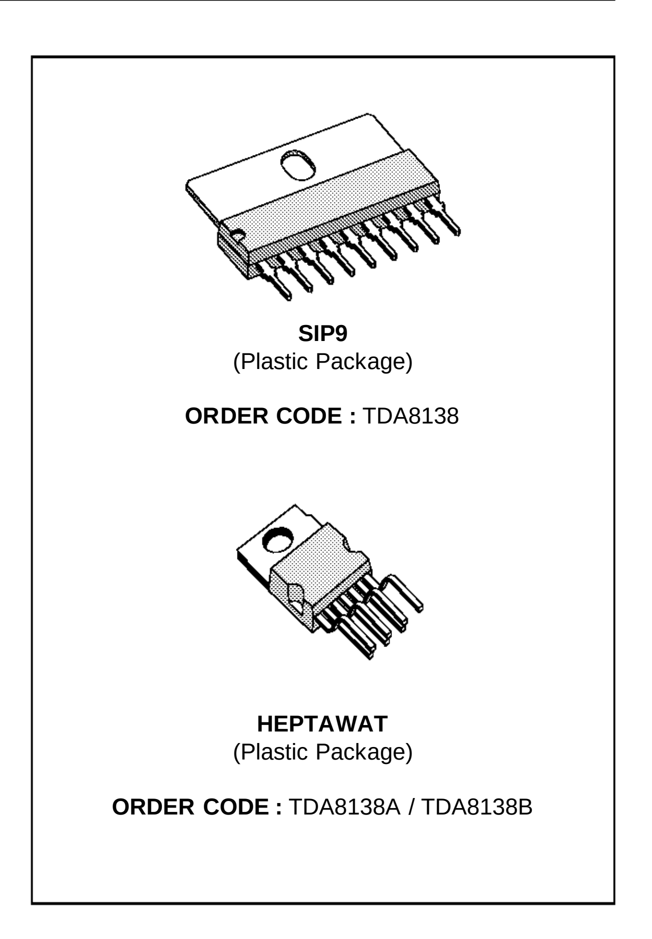


TDA8138

5.1V +12V REGULATOR WITH DISABLE AND RESET

- OUTPUT CURRENTS UP TO 1A
- FIXED PRECISION OUTPUT 1 VOLTAGE 5.1V +/- 2%
- FIXED PRECISION OUTPUT 2 VOLTAGE 12V +/- 2%
- OUTPUT 1 WITH RESET FACILITY
- OUTPUT 2 WITH DISABLE BY TTL INPUT
- SHORT CIRCUIT PROTECTION AT BOTH OUTPUTS
- THERMAL PROTECTION
- LOW DROP OUTPUT VOLTAGE
- AVAILABLE ALSO IN HEPTAWATT PACKAGE IN TWO VERSIONS : TDA8138A (DISABLE ONLY), TDA8138B (RESET ONLY)



DESCRIPTION

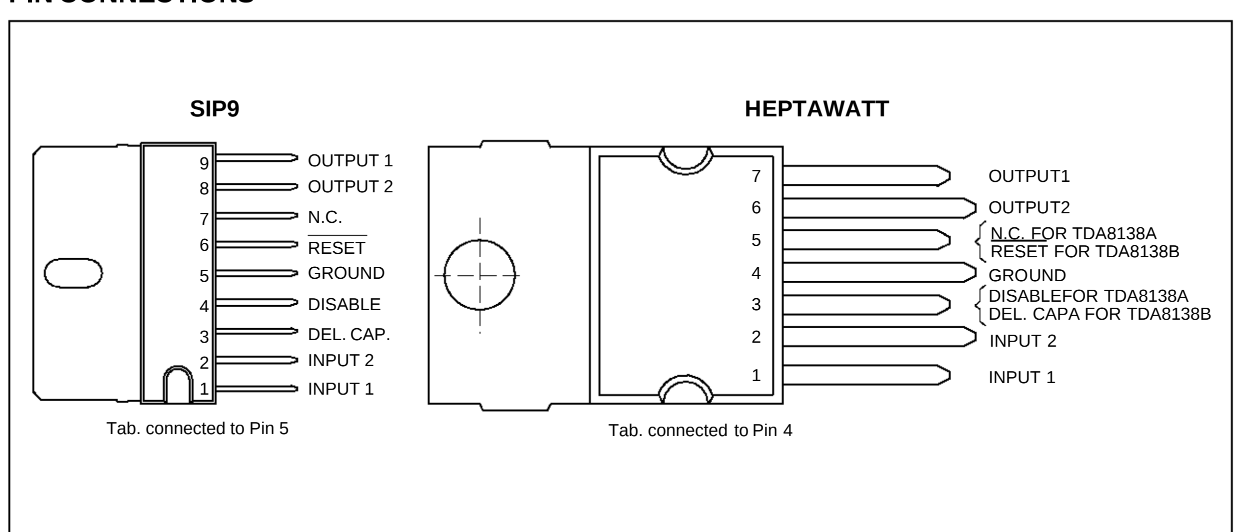
The TDA8138 is a monolithic dual positive voltage regulator designed to provide fixed precision output voltages of 5.1V and 12V at currents up to 1A.

An internal reset circuit generates a reset pulse when the output 1 decrease below the regulated voltage value (for TDA8138 and TDA8138B).

Output 2 can be disabled by TTL input (for TDA8138 and TDA8138A).

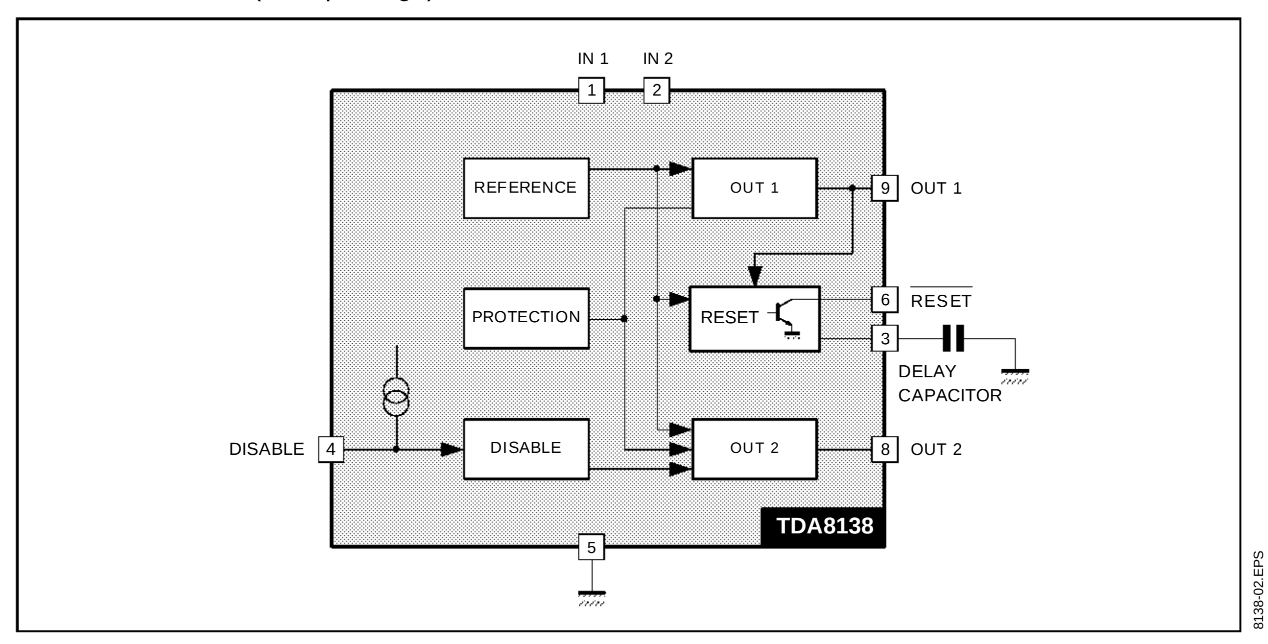
Short circuit and thermal protections are included in all the versions.

PIN CONNECTIONS



8138-01A.EPS - 8138-01B.EPS

BLOCK DIAGRAM (SIP9 package)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{IN}	DC Input Voltage Pin 1	20	V
V_{DIS}	Disable Input Voltage Pin 3 (Heptawatt) or Pin 4 (SIP9)	20	V
V_{RST}	Output Voltage at Pin 6 (SIP9) or Pin 5 (Heptawatt)	20	V
$I_{O1, 2}$	Output Currents	Internally Limited	
P_t	Power Dissipation	Internally Limited	
T_{stg}	Storage Temperature	-65 to +150	^oC
T_j	Junction Temperature	0 to +150	^oC

8138-01.TBL

THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{th\ (j-c)}$	Maximum Thermal Resistance Junction-case for SIP9 Maximum Thermal Resistance Junction-case for Heptawatt	8 3	$^oC/W$ $^oC/W$
$R_{th\ (j-a)}$	Maximum Thermal Resistance Junction-ambient for SIP9	60	$^oC/W$
T_j	Maximum Recommended Junction Temperature	130	^oC

8138-02.TBL

ELECTRICAL CHRACTERISTICS (V_{IN1} = 7V, V_{IN2} = 14V, T_j = 25°C, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{O1}	Output Voltage	I_{O1} = 10mA	5	5.1	5.2	V
V_{O2}	Output Voltage	I_{O2} = 10mA	11.76	12	12.24	V
V_{O1}	Output Voltage	7V < V_{IN1} < 14V 14 < V_{IN2} < 18V 5mA < $I_{O1,2}$ < 750mA	4.9		5.3	V
V_{O2}	Output Voltage		11.5		12.5	V
$V_{IO1,2}$	Dropout Voltage	$I_{O1,2}$ = 750mA $I_{O1,2}$ = 1A			1.4 2	V V
$V_{O1,2LI}$	Line Regulation	7V < V_{IN1} < 14V 14 < V_{IN2} < 18V $I_{O1,2}$ = 200mA			50 120	mV mV
$V_{O1,2LO}$	Load Regulation	5mA < I_{O1} < 0.6A 5mA < I_{O2} < 0.6A			100 250	mV mV
I_Q	Quiescent Current	I_{O1} = 10mA Output 2 Disabled			2	mA
V_{O1RST}	Reset Thrseshold Voltage	K = V_{O1}	K - 0.4	K - 0.25	K - 0.1	V
V_{RTH}	Reset Thrseshold Hysteresis	See circuit description	20	50	75	mV
t_{RD}	Reset Pulse Delay	C_e = 100nF See circuit description		25		ms
V_{RL}	Saturation Voltage in Reset Condition	I_5 = 5mA			0.4	V
I_{RH}	Leakage Current in Normal Condition (at Pin 6 for SIP9 or Pin 5 for Heptawatt)	V_5 = 10V			10	µA
$K_{O1,2}$	Output Voltage Thermal Drift	T_j = 0 to 125°C $K_O = \frac{\Delta V_O \cdot 10^6}{\Delta T \cdot V_O}$		100		ppm/°C
$I_{O1,2SC}$	Short Circuit Output Current	V_{IN1} = 7V, V_{IN2} = 14V $V_{IN1,2}$ = 16V (see Note)			1.6 1	A A
V_{DISH}	Disable Voltage High (out 2 active)		2			V
V_{DISL}	Disable Voltage Low (out 2 disabled)				0.8	V
I_{DIS}	Disable Bias Current	0V < V_{DIS} < 7V	-100		2	µA
T_{jsd}	Junction Temperature for Thermal Shut Down			145		°C

8138-03.TBL

Note : Safe permanent short-circuit is only guaranteed for input voltages up to 16V.

CIRCUIT DESCRIPTION

The TDA8138 is a dual voltage regulator with Reset and Disable (TD8138A : Disable only, TDA8138B : Reset only).

The two regulation parts are supplied from one voltage reference circuit trimmed by zener zap during EWS test.
Since the supply voltage of this last is connected at Pin 1 (V_{IN1}), the regulator 2 will not work if Pin 1 is not supplied.

The outputs stage have been realized in darlington configuration with a drop typical 1.2V.

The disable circuit, switch-off the output 2 if a voltage lower than 0.8V is applied at Pin 3 (Heptawatt) or Pin 4 (SIP9)

The Reset circuit checks the voltage at the output 1. If this one goes below V_{OUT} - 0.25V (4.85V typ.), the comparator ”a” (see Figure 1) discharges rapidly the capacitor C_e and the reset output goes at once Low. When the voltage at the out1 rises above V_{OUT} - 0.2V (4.9V typ.), the voltage V_{Ce} increases linearly to 2.5V corresponding to a delay td following the law : $t_1 = \frac{C_e \cdot 2.5V}{10\mu A}$ (see Figure 2), then the reset output goes high again. To avoid gliches in the reset output, the second comparator ”b” has a large hysteresis (1.9V).

Figure 1

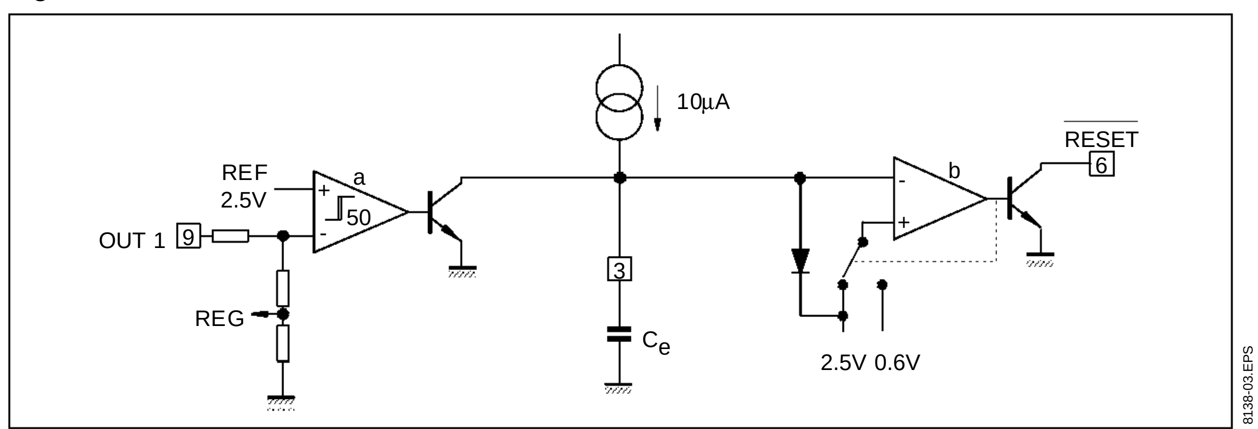
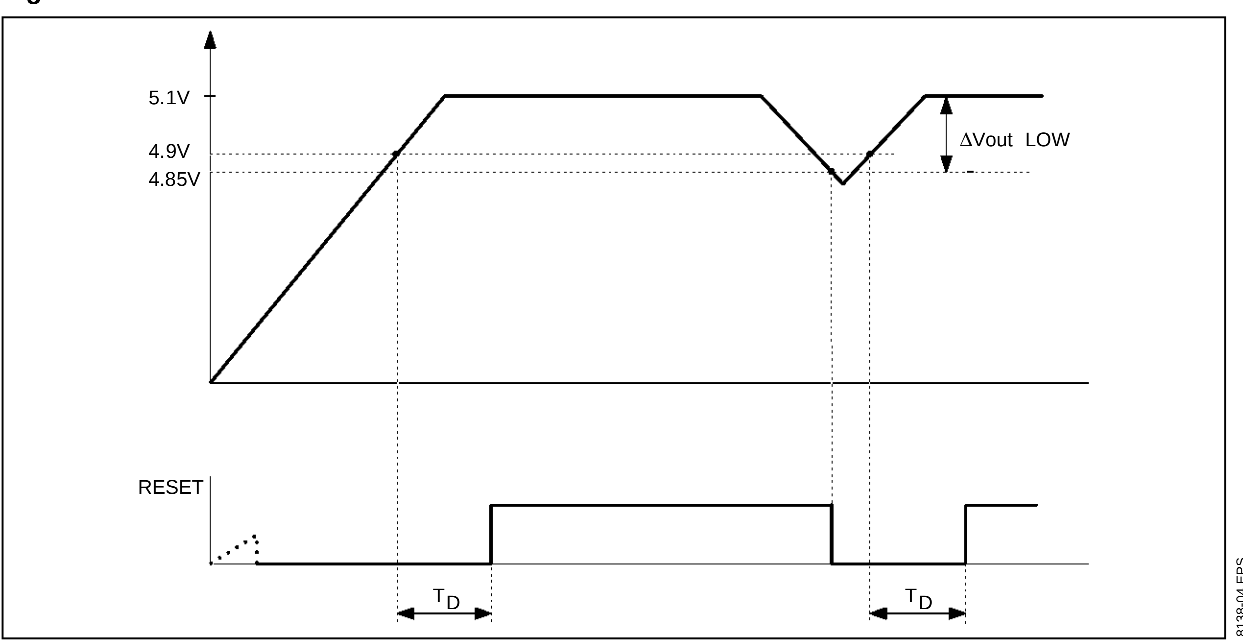
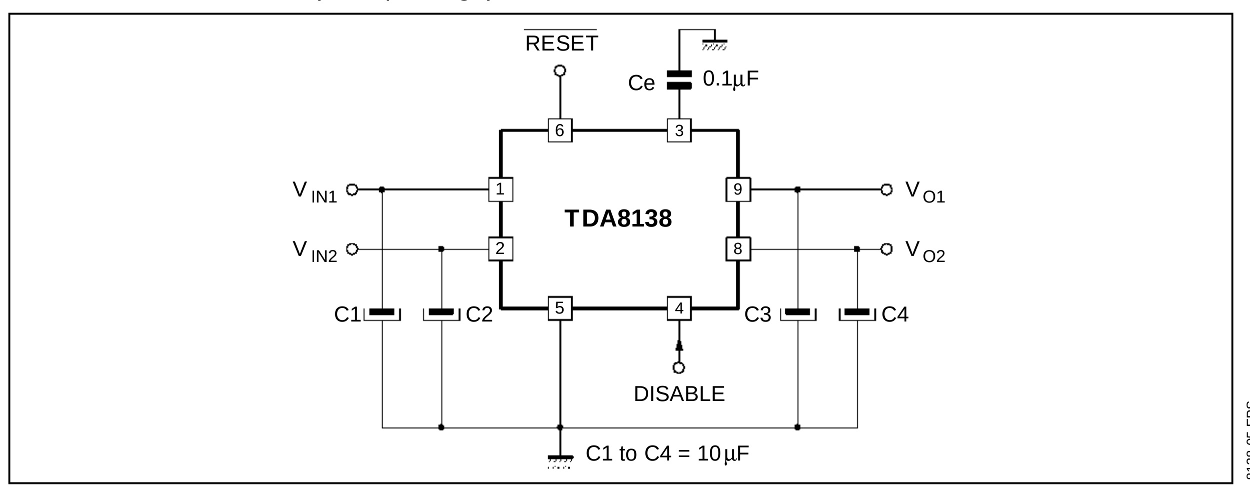


Figure 2

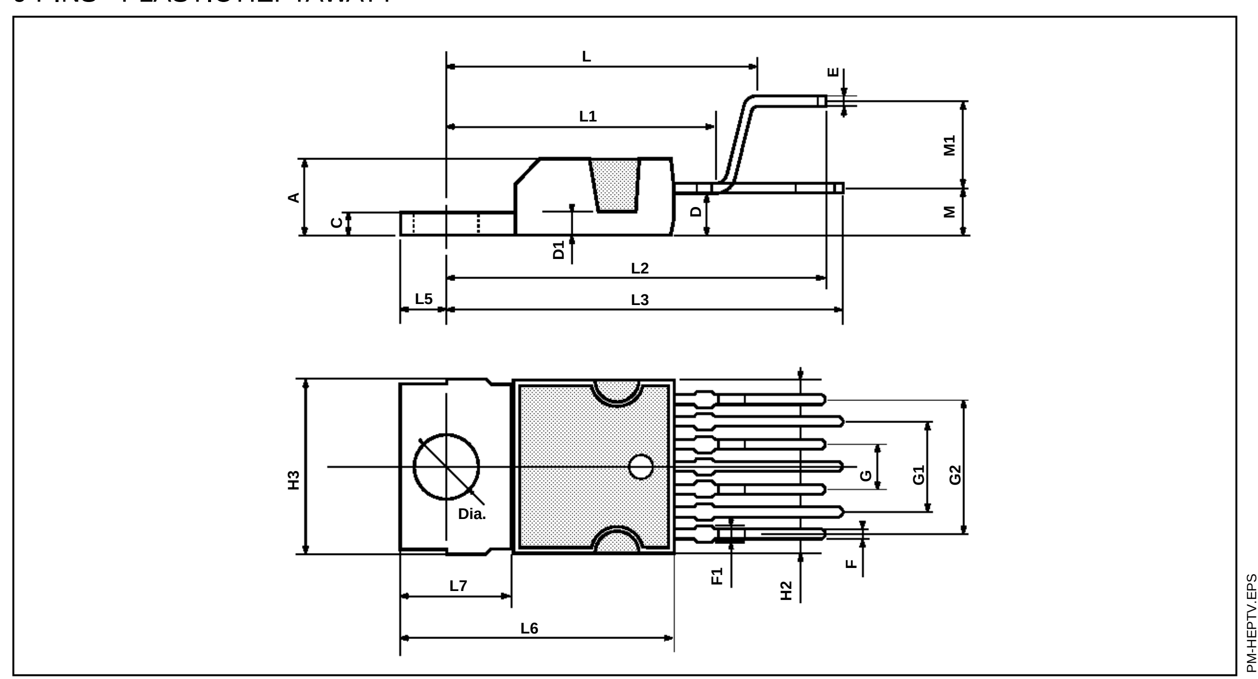


TYPICAL APPLICATION (SIP9 package)



PACKAGE MECHANICAL DATA

9 PINS - PLASTIC HEPTAWATT

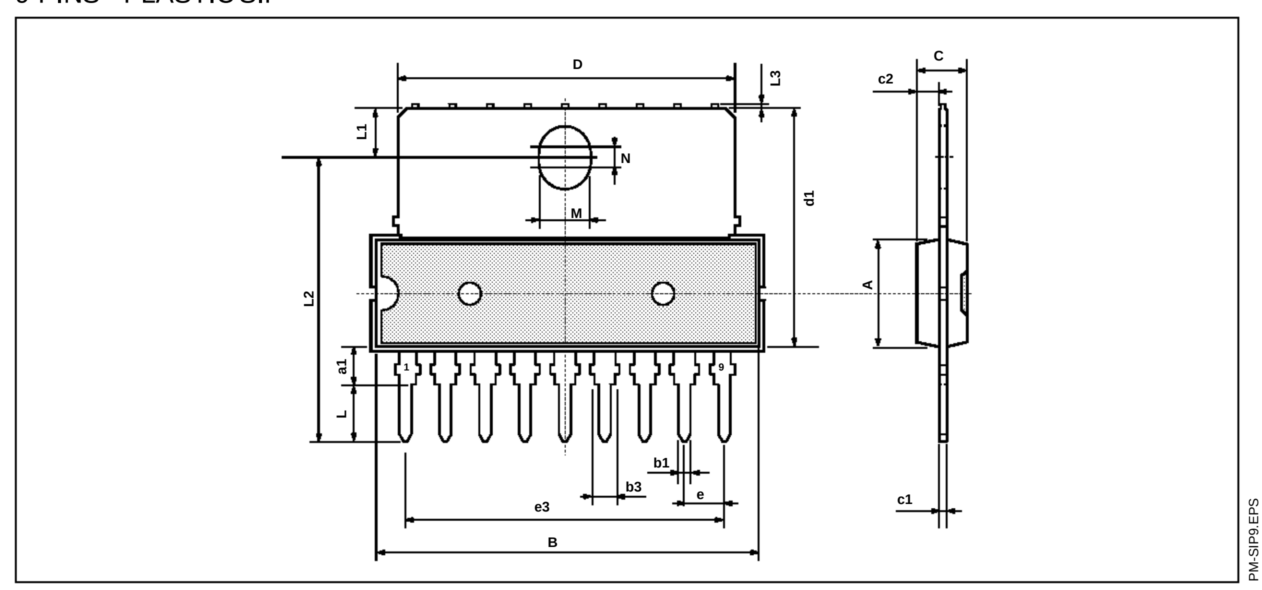


Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			4.8			0.189
C			1.37			0.054
D	2.4		2.8	0.094		0.110
D1	1.2		1.35	0.047		0.053
E	0.35		0.55	0.014		0.022
F	0.6		08	0.024		0.031
F1			0.9			0.035
G	2.41	2.54	2.67	0.095	0.100	0.105
G1	4.91	5.08	5.21	0.193	0.200	0.205
G2	7.49	7.62	7.8	0.295	0.300	0.307
H2			10.4			0.409
H3	10.05		10.4	0.396		0.409
L		16.97			0.668	
L1		14.92			0.587	
L2		21.54			0.848	
L3		22.62			0.891	
L5	2.6		3	0.102		0.118
L6	15.1		15.8	0.594		0.622
L7	6		6.6	0.236		0.260
M		2.8			0.110	
M1		5.08			0.200	
Dia.	3.65		3.85	0.144		0.152

HEPTV.TBL

PACKAGE MECHANICAL DATA

9 PINS - PLASTIC SIP



Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			7.1			0.280
a1	2.7		3	0.106		0.118
B			24.8			0.976
b1		0.5			0.020	
b3	0.85		1.6	0.033		0.063
C		3.3			0.130	
c1		0.43			0.017	
c2		1.32			0.052	
D			21.2			0.835
d1		14.5			0.571	
e		2.54			0.100	
e3		20.32			0.800	
L	3.1			0.122		
L1		3			0.118	
L2		17.6			0.693	
L3			0.25			0.010
M		3.2			0.126	

SIP9.TBL

